WHAT IS CLAIMED IS:

1. A CDMA decoder for decoding a CDMA encoded signal from a desired CDMA channel, comprising:

a receive input for receiving a CDMA encoded signal;

a code generator for generating a predetermined CDMA code for a predetermined CDMA channel that corresponds to an encoded signal encoded with a corresponding CDMA code transmitted over the predetermined CDMA channel;

a multiply/accumulate device for multiplying said received signal received on said receive input by said predetermined CDMA code word and operating in the analog domain, said multiply/accumulate device operable to accumulate the results of the multiplication operation over a symbol period to provide an analog result; and

a data conversion device for determining if the analog result corresponds to a predetermined digital state and, if so, generating a digital output corresponding to said predetermined digital state.

2. The CDMA decoder of Claim 1, wherein said predetermined digital state comprises multiple predetermined digital states and wherein said data conversion device is operable to generate multiple digital output states corresponding to the one of said multiple predetermined digital states to which the analog result has been determined to correspond.

3. The CDMA decoder of Claim 2, wherein said multiple predetermined digital states correspond to a "+1" logic state, a "0" logic state and a "-1" state.

4. The CDMA decoder of Claim 1, wherein said data conversion device, by the operation of generating said digital output, provides a correlation of said encoded signal with said generated code word for said associated CDMA channel.

5. The CDMA decoder of Claim 1, wherein said code generator operates in synchronization with a chip clock such that said predetermined CDMA code word is clocked by said chip clock, which chip clock changes from one logic state to a second logic state, and said multiply/accumulation device further including a blanking device for blanking the operation of said multiply/accumulation device during at least one of the leading or lagging edges of said chip clock at said one logic state for a predetermined blanking duration during which the operation of said multiply/accumulation device is inhibited to prevent accumulation of information therefrom.

6. The CDMA decoder of Claim 5, wherein said blanking device operates during said leading and lagging edges of the chip clock.

7. The CDMA decoder of Claim 1, and further comprising a blanking device for blanking the operation of said multiply/accumulation device for at least one of the leading or the lagging edges of said received signal for a predetermined blanking duration when transitioning between logic states.

8. The CDMA decoder of Claim 7, wherein said blanking device is operable to blank said operation of said multiply/accumulation device for both said leading and lagging edges for said predetermined blanking duration.

9. The CDMA decoder of Claim 1, wherein said code generator is operable to generate a plurality of CDMA codes, each associated with one of a plurality of CDMA channels such that said received input can receive a plurality of CDMA encoded signals each on a different channel and further comprising a plurality of multiply/accumulate devices, one for each channel and for each code word generated by said code generator and wherein said data conversion device is operable to determine for each of the multiply/accumulation devices if the associated analog result corresponds to said predetermined digital state and if so, generating a digital output corresponding to the

associated multiply/accumulation device such that a digital output is provided for each of said multiply/accumulation devices.

10. The CDMA decoder of Claim 9 and further comprising a subtraction device for subtracting from the analog result output from each of said multiply/accumulation devices contributions from signals on selective one of the other channels encoded with their associated CDMA codes.

11. The CDMA decoder of Claim 10, wherein said subtraction device comprises:

a table device for storing defined predetermined relationships between the output of each of said multiply/accumulation devices for a signal input thereto on its associated channel and the output therefrom for signals input thereto for selected other channels, said relationship comprising a scale factor for the analog result;

a multiplication device associated with each of said multiplication devices for multiplying the determined digital state from the other of said selected channels output by said associated data conversion device from siad multiply/accumulation devices for said selected other channels; and

a summation device for subtracting the output of each of said multiplication devices from said analog result of said each multiply/accumulation device prior to input to said data conversion device associated with said each multiply/accumulation device.

12. The CDMA decoder of Claim 9, and further comprising an automatic gain control device for adjusting the gain of each of said multiply/accumulation devices to compensate for gain errors therein.

13. The CDMA decoder of Claim 12, wherein said automatic gain control device comprises:

a multiplexer device for operating in a calibration mode and selecting one of said code words generated by said code generator associated with a reference one of the CDMA channels for input to each of said multiply/accumulation devices;

a gain control device for adjusting the gain on the output of each of said multiply/accumulation devices such that, for the signal received on the reference one of the CDMA channels associated with the given one of said code words, the output signal level can be adjusted to a substantially similar level compared to the remaining multiply/accumulation devices; and

a storage device for storing the determined gain parameters for each of said multiply/accumulation devices.

14. The CDMA decoder of Claim 1, wherein said multiply/accumulation device comprises:

at least one series leg including first and second series connected transistors disposed between a first node and a second reference voltage, said first transistor having the gate thereof connected to the received signal on said receive input and the gate of said second transistor connected to receive said associated code word;

a storage device connected to said first node;

a precharge device for enabling said first node to be precharged to a defined level prior to the initiation of the accumulation operation at the beginning of a symbol period; and

wherein said first and second transistors provide a multiplication operation for said code word and the received signal and said storage device is operable to accumulate the results of the multiplication operation over a symbol period.

15. The CDMA decoder of Claim 14, wherein said multiply/accumulation device operates in a differential mode and further comprising a second leg comprised of first and second transistors connected in series between a second node and said reference voltage;

a storage device connected to said second node; and

the gate of said first transistor in said second leg connected to said receive signal on said receive input and the gate of said second transistor connected to the inverse of said associated code word, wherein the differential voltage between said first and second nodes comprises the analog result.

16. A method for decoding a CDMA encoded signal from a desired CDMA channel, comprised the steps of:

receiving the CDMA encoded signal on a receive input;

generating a predetermined CDMA code for a predetermined CDMA channel that corresponds to an encoded signal encoded with a corresponding CDMA code transmitted over the predetermined CDMA channel;

multiplying the received signal received on the receive input by the predetermined CDMA code word in the analog domain and accumulating the results of the multiplication operation over a symbol period to provide an analog result; and

determining if the analog result corresponds to a predetermined digital state and, if so, generating a digital output corresponding to the predetermined digital state.

17. The method of Claim 16, wherein the predetermine digital state comprises multiple predetermined digital states, and wherein the step of generating a digital output is operable to generate multiple digital output states, each corresponding to the one of the multiple predetermined digital states to which the analog result has been determined to correspond.

18. The method of Claim 16, wherein the step of generating the code word is operable to generate a sequence of logic states that are synchronized with a chip clock such that the predetermined CDMA code word is comprised of a plurality of logic states that are clocked by the chip clock, which chip clock changes from one logic state to a second logic state and the step of multiplying and the step of accumulating further including the step of blanking the operation of multiplying and accumulating during at least one of the leading or lagging edges of the chip clock at the one logic state for a predetermined blanking duration during which the multiplying and accumulation steps are inhibited to prevent accumulation of information therefrom.

19. The method of Claim 18, wherein the step of blanking operates only during the leading and lagging edges of the chip clock.

20. The method of Claim 16, wherein the step of generating the predetermined CDMA code is operable to generate a plurality of CDMA codes, each associated with one of a plurality of CDMA channels such that the receive input can receive a plurality of CDMA encoded signals each on a different channel and further comprising the step of providing a plurality of multiply/accumulation devices, each for carrying out the multiplying and accumulation steps for a given one of the CDMA channels and wherein the step of determining for each of the multiply/accumulation devices is operable to determine if the associated analog result corresponds to the predetermined digital state and, if so, generating a digital output corresponding to the associated multiply/accumulation device such that a digital output is provided for each of the multiply/accumulation devices.

21. The method of Claim 20, and further comprising the step of subtracting from the analog result output from each of the multiply/accumulation devices contributions from signals on selective ones of the other channels encoded with their associated CDMA codes.